JEDEC STANDARD

Standard for Definition of ‘CU878 PLL Clock Driver for Registered DDR2 DIMM Applications

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STANDARD FOR DEFINITION OF ’CU878 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS

(Formerly JEDEC Board Ballot JCB-04-56A, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a ’CU878 PLL clock device for registered DDR2 DIMM applications.

The purpose is to provide a standard for a ’CU878 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Definitions for the purpose of this document

$C_{I(\Delta)}$ – Delta input capacitance.

3 Device standard

3.1 Description

This PLL Clock Buffer is designed for a V_{DDQ} of 1.8 V, an AV_{DD} of 1.8 V and differential data input and output levels. Package options include a plastic 52-ball VFBGA and a 40-pin MLF.

The device is a zero delay buffer that distributes a differential clock input pair (CK, $\overline{\text{CK}}$) to ten differential pair of clock outputs (Y[0:9], $\overline{\text{Y[0:9]}}$) and one differential pair feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the input clocks (CK, $\overline{\text{CK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), the LVCMOS (OE, OS) and the Analog Power input (AV_{DD}). When OE is low, the outputs (except FBOUT/$\overline{\text{FBOUT}}$) are disabled while the internal PLL continues to maintain its locked-in frequency. OS (Output Select) is a program pin that must be tied to GND or V_{DDQ}. When OS is high, OE will function as described above. When OS is low, OE has no effect on Y7/$\overline{\text{Y7}}$ (they are free running in addition to FBOUT/$\overline{\text{FBOUT}}$). When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When both clock signals (CK, $\overline{\text{CK}}$) are logic low, the device will enter a low power mode. An input logic detection circuit on the differential inputs, independent from the input buffers, will detect the logic low level and perform a low power state where all outputs, the feedback and the PLL are OFF. When the inputs transition from both being logic low to being differential signals, the PLL will be turned back on, the inputs and outputs will be enabled and the PLL will obtain phase lock between the feedback clock pair (FBIN, $\overline{\text{FBIN}}$) and the input clock pair (CK, $\overline{\text{CK}}$) within the specified stabilization time t_L.

The PLL in the ’CU878 clock driver uses the input clocks (CK, $\overline{\text{CK}}$) and the feedback clocks (FBIN, $\overline{\text{FBIN}}$) to provide high-performance, low-skew, low-jitter output differential clocks (Y[0:9], $\overline{\text{Y[0:9]}}$). The ’CU878 is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

The ’CU878 is characterized for operation from 0 ^{o}C to 70 ^{o}C.

3.1 Description (cont'd)

Topview

BGA

	1	2	3	4	5	6
A	Y1	Y0	$\overline{Y0}$	$\overline{Y5}$	Y5	Y6
B	$\overline{Y1}$	GND	GND	GND	GND	$\overline{Y6}$
C	$\overline{Y2}$	GND	NB	NB	GND	$\overline{Y7}$
D	Y2	VDDQ	VDDQ	VDDQ	OS	Y7
E	CK	VDDQ	NB	NB	VDDQ	Fbin
F	$\overline{CK}$	VDDQ	NB	NB	OE	$\overline{Fbin}$
G	AGND	VDDQ	VDDQ	VDDQ	VDDQ	$\overline{Fbout}$
H	AVDD	GND	NB	NB	GND	Fbout
J	Y3	GND	GND	GND	GND	Y8
K	$\overline{Y3}$	$\overline{Y4}$	Y4	Y9	$\overline{Y9}$	$\overline{Y8}$

Figure 1 — 52-Ball VF-BGA (10x6 Array, 7.0x4.5 mm Body Size, 0.65 mm Pitch, MO-225 Variation BA) package pinouts

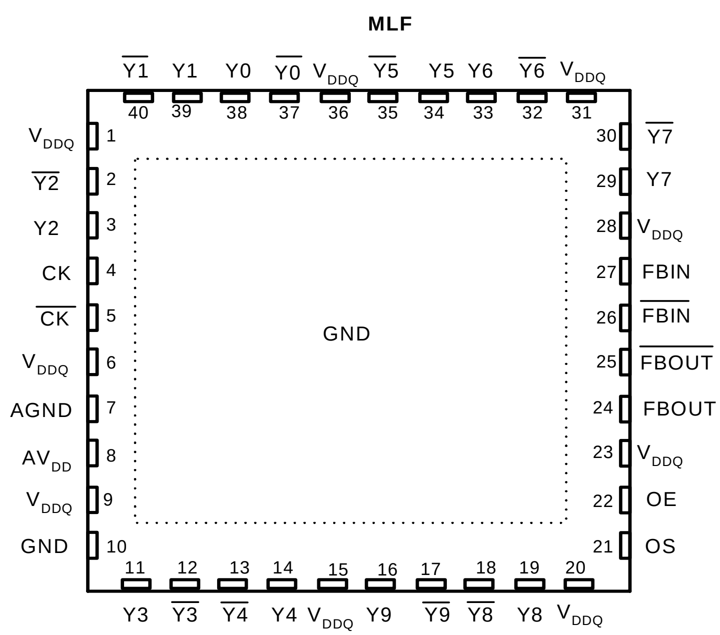


Figure 2 — 40-pin HP-VFQFP-N (6.0x6.0 mm Body Size, 0.5 mm Pitch, MO-220, variation VJJD-2, E2 & D2 nominal = 2.9 mm +/- 0.15 mm) package pinouts

3.2 Terminal functions

Table 1 — Terminal Functions

Terminal Name	Description	Electrical Characteristics
AGND	Analog Ground	Ground
AV_{DD}	Analog power	1.8 V nominal
CK	Clock input with a (10K-100K Ohm) pulldown resistor	Differential input
$\overline{\text{CK}}$	Complementary clock input with a (10K-100K Ohm) pulldown resistor	Differential input
FBIN	Feedback clock input	Differential input
$\overline{\text{FBIN}}$	Complementary feedback clock input	Differential input
FBOUT	Feedback clock output	Differential output
$\overline{\text{FBOUT}}$	Complementary feedback clock output	Differential output
OE	Output Enable (Asynch)	LVCMOS input
OS	Output Select (tied to GND or V_{DDQ})	LVCMOS input
GND	Ground	Ground
V_{DDQ}	Logic and output power	1.8 V nominal
Y[0:9]	Clock outputs	Differential outputs
$\overline{\text{Y[0:9]}}$	Complementary clock outputs	Differential outputs
NB	No ball	

3.3 Function table

Table 2 — Function table

Inputs					Outputs				PLL
AV_{DD}	OE	OS	CK	$\overline{\text{CK}}$	Y	$\overline{\text{Y}}$	FBOUT	$\overline{\text{FBOUT}}$	
GND	H	X	L	H	L	H	L	H	Bypassed/ Off
GND	H	X	H	L	H	L	H	L	Bypassed/ Off
GND	L	H	L	H	$*L_{(Z)}$	$*L_{(Z)}$	L	H	Bypassed/ Off
GND	L	L	H	L	$*L_{(Z)}$, Y7 active	$*L_{(Z)}$, $\overline{\text{Y7}}$ active	H	L	Bypassed/ Off
1.8V(nom)	L	H	L	H	$*L_{(Z)}$	$*L_{(Z)}$	L	H	On
1.8V(nom)	L	L	H	L	$*L_{(Z)}$, Y7 active	$*L_{(Z)}$, $\overline{\text{Y7}}$ active	H	L	On
1.8V(nom)	H	X	L	H	L	H	L	H	On
1.8V(nom)	H	X	H	L	H	L	H	L	On
1.8V(nom)	X	X	L	L	$*L_{(Z)}$	$*L_{(Z)}$	$*L_{(Z)}$	$*L_{(Z)}$	Off
1.8V(nom)	X	X	H	H	Reserved				

* $L_{(Z)}$ means the outputs are disabled to a low state meeting the I_{ODL} limit in Table 5.

3.4 Logic diagram

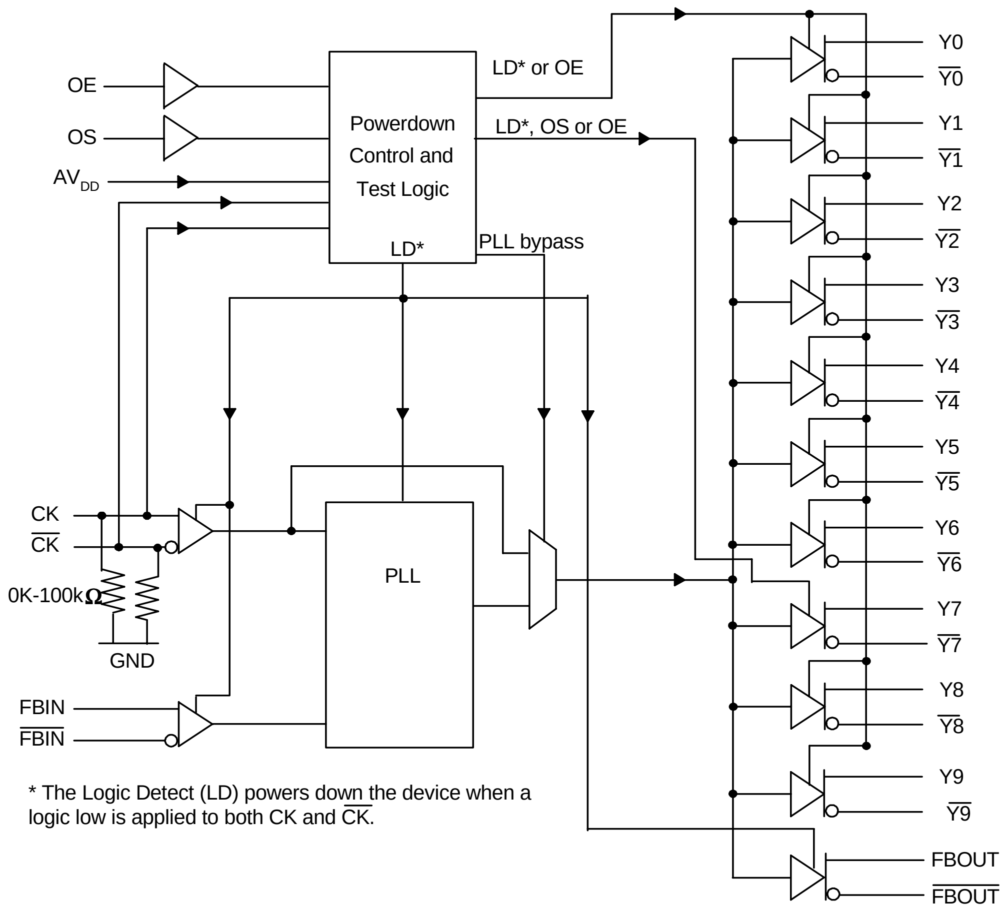


Figure 3 — Logic diagram (positive logic)

3.5 Absolute maximum ratings

Table 3 — Absolute maximum ratings over operating free-air temperature range (see Note 1)

Supply voltage range, V_{DDQ} or AV_{DD}	–0.5 V to 2.5 V
Input voltage range, V_I (see Notes 2 and 3)	–0.5 to V_{DDQ} + 0.5 V
Output voltage range, V_O (see Notes 2 and 3)	–0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DDQ}$)	±50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDQ}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	±50 mA
Continuous current through each V_{DDQ} or GND	±100 mA
Storage temperature range, T_{STG}	–65 °C to 150 °C

NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3 This value is limited to 2.5 V maximum.

3.6 Recommended operating conditions

Table 4 — Recommended operating conditions (see Note 1)

			Min	Nom	Max	Unit
V_{DDQ}	Output supply voltage		1.7	1.8	1.9	V
AV_{DD}	Supply voltage	See Note 1		V_{DDQ}		
V_{IL}	Low-level input voltage, see Note 2	OE, $\overline{OS}$, CK, $\overline{CK}$			0.35 x V_{DDQ}	V
V_{IH}	High-level input voltage, see Note 2	OE, $\overline{OS}$, CK, $\overline{CK}$	0.65 x V_{DDQ}			V
I_{OH}	High-level output current, See Figure 5				- 9	mA
I_{OL}	Low-level output current, See Figure 5				9	mA
V_{IX}	Input differential-pair cross voltage		(V_{DDQ}/2)-0.15		(V_{DDQ}/2)+0.15	V
V_{IN}	Input voltage level		- 0.3		V_{DDQ} + 0.3	V
V_{ID}	Input differential voltage, See Note 2 and Figure 12	DC	0.3		V_{DDQ} + 0.4	V
		AC	0.6		V_{DDQ} + 0.4	**V**
T_A	Operating free-air temperature		0		70	**°C**

NOTE 1 The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operationing conditions and no timing parameters are guaranteed.

NOTE 2 V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$, see Figure 12 for definition. For CK and $\overline{CK}$ the V_{IH} and V_{IL} limits are used to define the DC low and high levels for the logic detect state.

3.7 DC specifications

Table 5 — Electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	AV_{DD}, V_{DDQ}	MIN	TYP	MAX	UNIT
V_{IK}	All inputs	I_I = –18 mA	1.7 V			-1.2	V
V_{OH}	High output voltage	I_{OH} = –100 µA	1.7 to 1.9 V	V_{DDQ}-0.2			V
		I_{OH} = –9 mA	1.7 V	1.1			
V_{OL}	Low output voltage	I_{OL} = 100 µA	1.7 to 1.9 V			0.1	V
		I_{OL} = 9 mA	1.7 V			0.6	
I_{ODL}	Output disabled low current	OE = L, V_{ODL} = 100mV	1.7 V	100			µA
V_{OD}	Output differential voltage, the magnitude of the difference between the true and complimentary outputs, see Figure 12 for definition.		1.7 V	0.6			V
I_I	CK, $\overline{CK}$	$V_I = V_{DDQ}$ or GND	1.9 V			± 250	µA
	OE, OS, FBIN, $\overline{FBIN}$	$V_I = V_{DDQ}$ or GND	1.9 V			± 10	
I_{DDLD}	Static supply current, $I_{DDQ} + I_{ADD}$	CK and $\overline{CK}$ = L	1.9 V			500	µA
I_{DD}	Dynamic supply current, $I_{DDQ} + I_{ADD}$, see Note 1 for C_{PD} calculation	CK and $\overline{CK}$ = 270 MHz, all outputs are open (not connected to a PCB)	1.9 V			300	mA
C_I	CK and $\overline{CK}$	$V_I = V_{DDQ}$ or GND	1.8 V	2		3	pF
	FBIN and $\overline{FBIN}$	$V_I = V_{DDQ}$ or GND		2		3	
$C_{I(\Delta)}$	CK and $\overline{CK}$	$V_I = V_{DDQ}$ or GND				0.25	
	FBIN and $\overline{FBIN}$	$V_I = V_{DDQ}$ or GND				0.25	

NOTE 1 Total $I_{DD} = I_{DDQ}+I_{ADD} = F_{CK} * C_{PD} * V_{DDQ}$, solving for $C_{PD} = (I_{DDQ}+I_{ADD})/(F_{CK}*V_{DDQ})$ where F_{CK} is the input Frequency, V_{DDQ} is the power supply and C_{PD} is the Power Dissipation Capacitance.

3.8 Timing requirements

Table 6 — Timing requirements over recommended operating free-air temperature range.

		AV_{DD}, V_{DDQ} = 1.8 V ± 0.1 V		UNIT
		MIN	MAX	
f_{CK}	Operating clock frequency (see Notes 1 and 2)	125	270	MHz
	Application clock frequency (see Notes 1 and 3)	160	270	MHz
t_{DC}	Input clock duty cycle	40	60	%
t_L	Stabilization time (see Note 4)		6	μs

NOTE 1 The PLL must be able to handle spread spectrum induced skew.

NOTE 2 Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)

NOTE 3 Application clock frequency indicates a range over which the PLL must meet all timing parameters.

NOTE 4 Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and $\overline{CK}$ go to a logic low state, enter the power-down mode and later return to active operation. CK and $\overline{CK}$ may be left floating after they have been driven low for one complete clock cycle.

3.9 AC specifications

Table 7 — Switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 7)

PARAMETER	DESCRIPTION	Diagram	AV_{DD}, V_{DDQ} = 1.8 V ± 0.1 V			UNIT
			MIN	Nom	MAX	
t_{en}	OE to any Y/$\overline{\text{Y}}$	see Figure 14			8	ns
t_{dis}	OE to any Y/$\overline{\text{Y}}$	see Figure 14			8	ns
$t$jit(cc+)	Cycle-to-cycle period jitter	see Figure 7	0		40	ps
$t$jit(cc-)			0		-40	ps
$t_{(\varnothing)}$	Static phase offset (see Note 1)	see Figure 8	-50		50	ps
$t_{(\varnothing)dyn}$	Dynamic phase offset	see Figure 13	-50		50	ps
$t$sk(o)	Output clock skew	see Figure 9			40	ps
$t$jit(per)	Period jitter (see Note 2)	see Figure 10	-40		40	ps
$t$jit(hper)	Half-period jitter (see Note 2, 4)	see Figure 11	-75		75	ps
slr(i)	Output Enable (OE)	see Figure 12	0.5			V/ns
	Input clock slew rate, measured single ended.	see Figure 12	1	2.5	4	V/ns
slr(o)	Output clock slew rate, measured single ended. (see Note 3, 6)	see Figures 4 and 12	1.5	2.5	3	V/ns
V_{OX}	Output differential-pair cross-voltage, See Note 5	see Figure 5	(V_{DDQ}/2) - 0.1		(V_{DDQ}/2) + 0.1	V
The PLL in the ’CU878 must be capable of meeting all the above test parameters while supporting SSC synthesizers with the following parameters:						
	SSC modulation frequency		30.00		33	kHz
	SSC clock input frequency deviation		0.00		–0.50	%
’CU878 PLL designs should target the values below to minimize the SSC induced skew:						
	PLL Loop bandwidth (-3 dB from unity gain)		2.0			MHz

NOTE 1 Static Phase Offset does not include Jitter.

NOTE 2 Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.

NOTE 3 The Output Slew Rate is determined from the IBIS model into the load shown in Figure 4. It is measured single ended.

NOTE 4 Design Target is 60ps, unless it is unacheivable.

NOTE 5 V_{OX} specified at the DRAM clock input or the test load.

NOTE 6 To eliminate the impact of input slew rates on static phase offset, the input slew rates of Reference Clock Input CK,$\overline{\text{CK}}$ and Feedback Clock Input FBIN, $\overline{\text{FBIN}}$ are recommended to be nearly equal. The 2.5 V/ns slew rates are shown as a recommended target. Compliance with these Nom values is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR2 DIMM application.

NOTE 7 There are two different terminations that are used with the above ac tests. The load/board in Figure 5 is used to measure the input and output differential-pair cross-voltage only. The load/board in Figure 6 is used to measure all other tests. For consistency, equal length cables should be used.

4 Output Buffer Characteristics

4.1 Purpose

The following table describes output-buffer Voltage vs. Current (V/I) characteristics that are sufficient to meet the requirements of registered DDR2 DIMM performance and timings. These curves are generated from the IBIS pull-up and pull-down data. Figure 4 shows the test condition used to generate this data. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. These curves are target goals and will be finalized after initial silicon is available.

Table 8 — Output Buffer Voltage vs. Current (V/I) Characteristics

	Pull-Down		Pull-Up	
Voltage (V)	I(mA) MIN	I(mA) MAX	I(mA) MIN	I(mA) MAX
-0.6	-16.4	-56.1	14.5	55.0
-0.5	-11.2	-43.2	11.4	45.1
-0.4	-8.4	-33.5	9	35.6
-0.3	-6.2	-25.3	6.7	26.4
-0.2	-4.1	-17.1	4.4	17.3
-0.1	-2.1	-8.7	2.2	8.5
0	0	0.0	0	0.0
0.1	2	8.4	-2.1	-8.1
0.2	4	16.2	-4.1	-15.8
0.3	5.8	23.2	-6	-23.0
0.4	7.5	29.6	-7.7	-29.8
0.5	9	35.2	-9.3	-36.0
0.6	10.4	40.1	-10.7	-41.6
0.7	11.5	44.2	-11.9	-46.7
0.8	12.3	47.5	-12.8	-51.2
0.9	12.9	50.0	-13.5	-55.1
1.0	13.2	51.5	-13.9	-58.3
1.1	13.4	52.4	-14.2	-61.0
1.2	13.6	52.9	-14.3	-63.0
1.3	13.7	53.2	-14.5	-64.5
1.4	13.7	53.5	-14.6	-65.7
1.5	13.8	53.7	-14.6	-66.5
1.6	13.8	53.8	-14.7	-67.2
1.7	13.9	53.9	-14.8	-67.8
1.8	13.9	54.0	-14.8	-68.4
1.9	14	54.1	-14.9	-68.9
2.0	14	54.2	-14.9	-69.4
2.1	14.1	54.3	-15	-69.8
2.2	14.2	54.3	-15.1	-70.3
2.3	14.8	54.4	-16.1	-71.0
2.4	17	54.7	-20.3	-74.0

5 Test circuit and switching waveforms

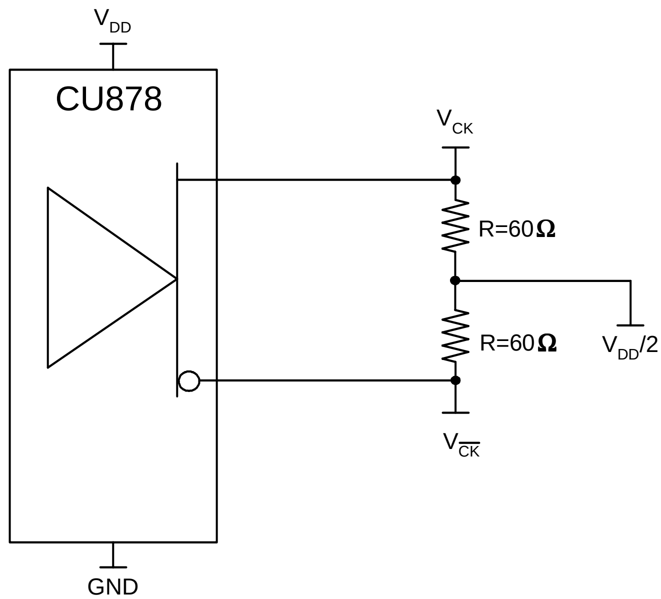


Figure 4 — IBIS Model Output Load

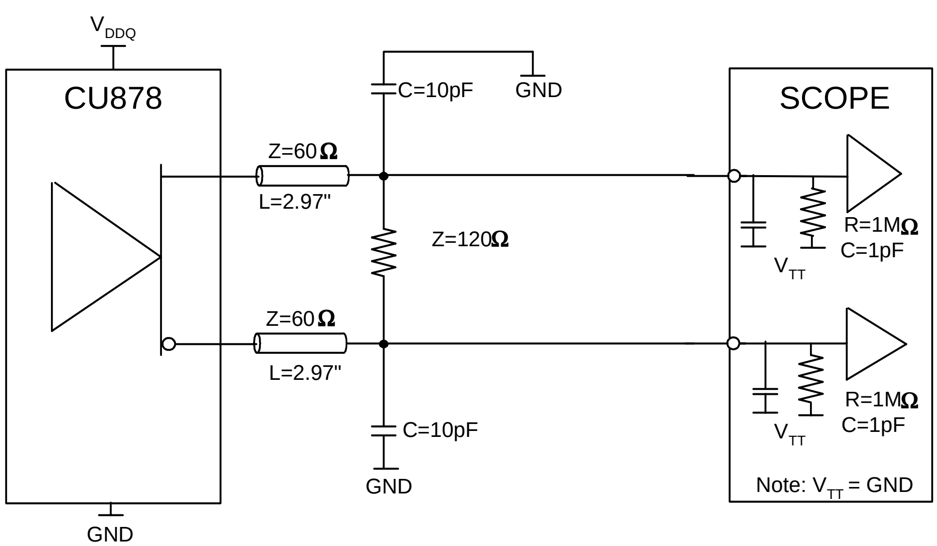


Figure 5 — Output Load Test Circuit1

5 Test circuit and switching waveforms (cont'd)

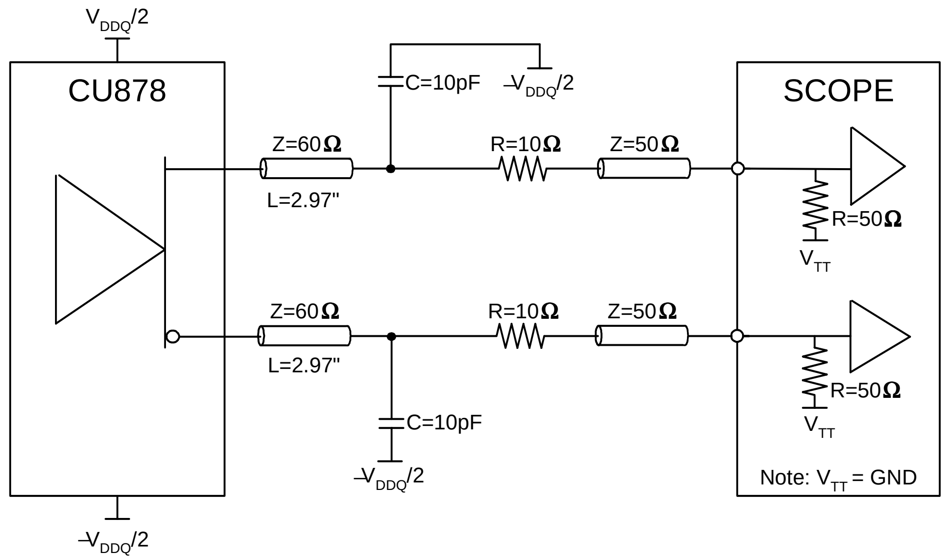


Figure 6 — Output Load Test Circuit2

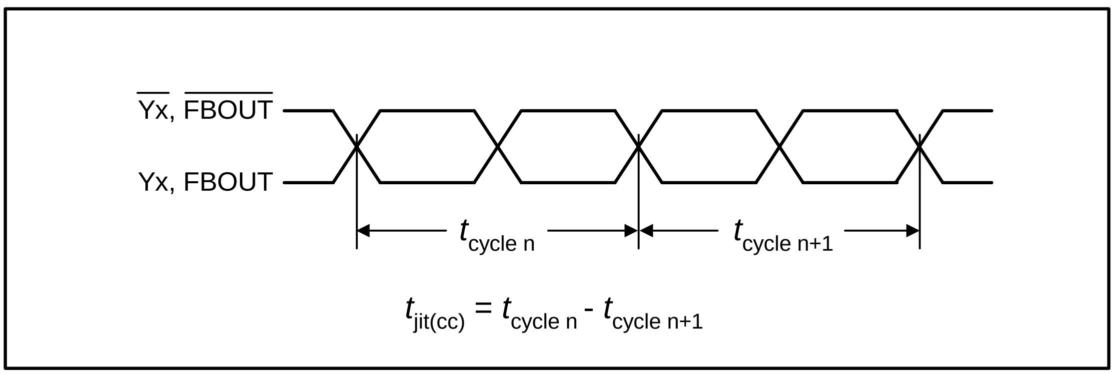
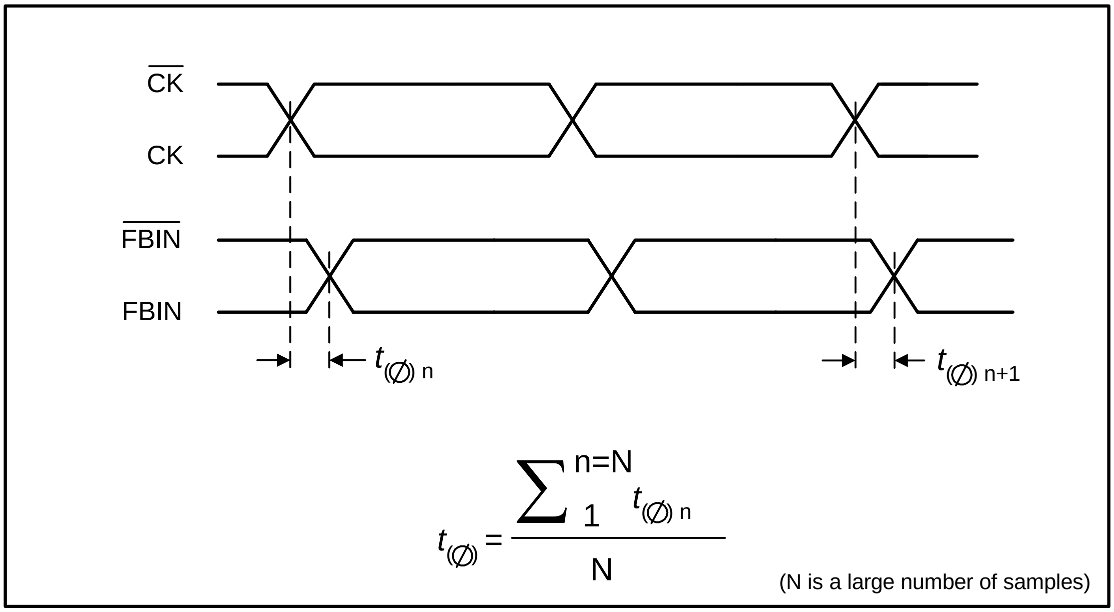


Figure 7 — Cycle-to-Cycle Period Jitter

5 Test circuit and switching waveforms (cont'd)



(N>1000 samples)

Figure 8 — Static Phase Offset

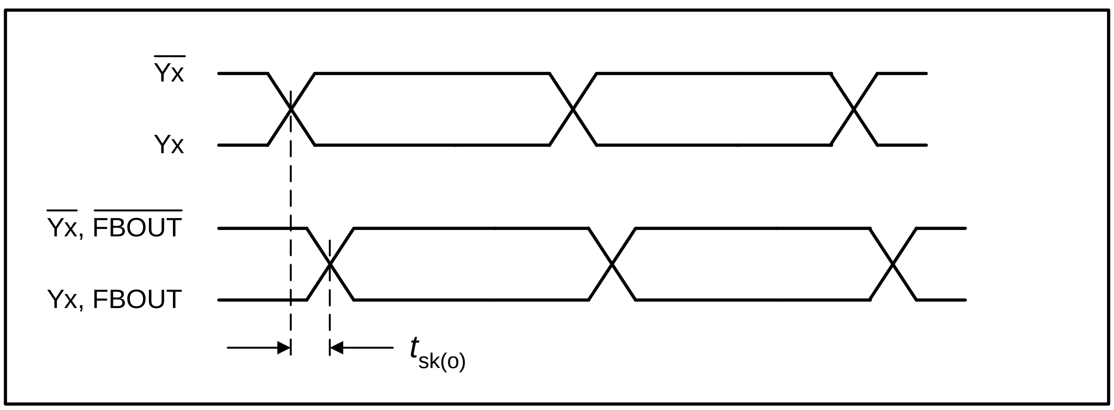
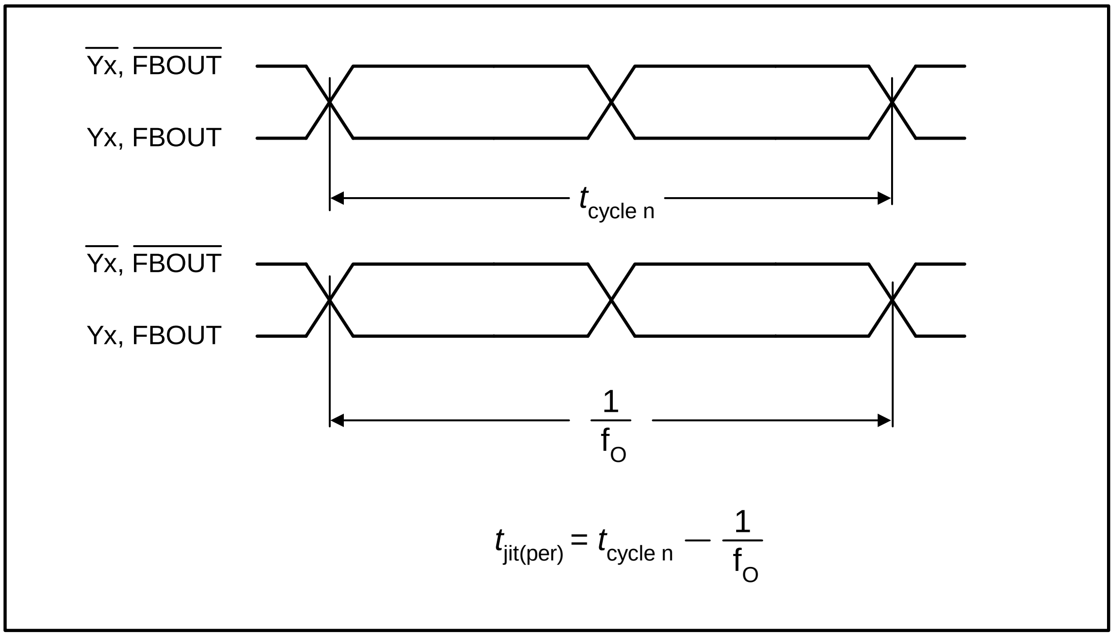


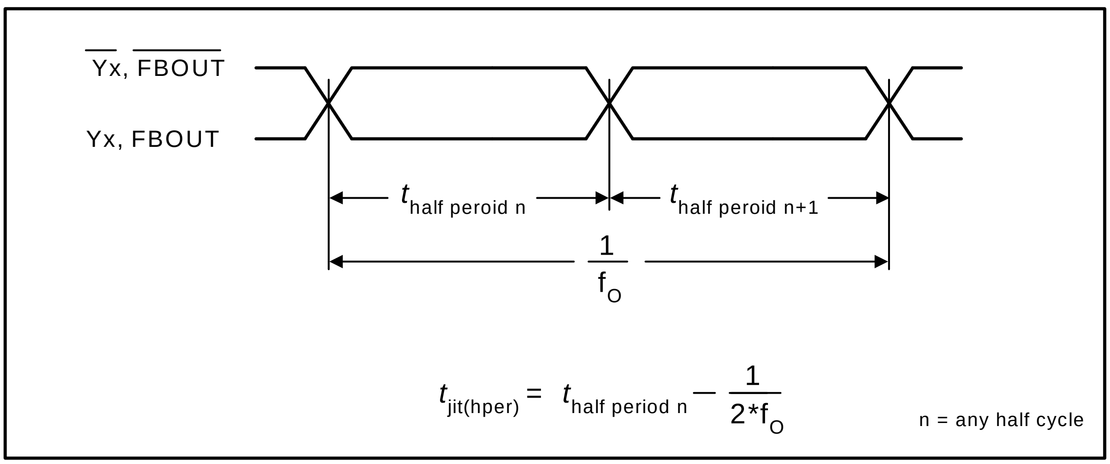
Figure 9 — Output Skew

5 Test circuit and switching waveforms (cont'd)



(f_O = average input frequency measured at CK/$\overline{CK}$)

Figure 10 — Period Jitter



(f_O = average input frequency measured at CK/$\overline{CK}$)

Figure 11 — Half-Period Jitter

5 Test circuit and switching waveforms (cont'd)

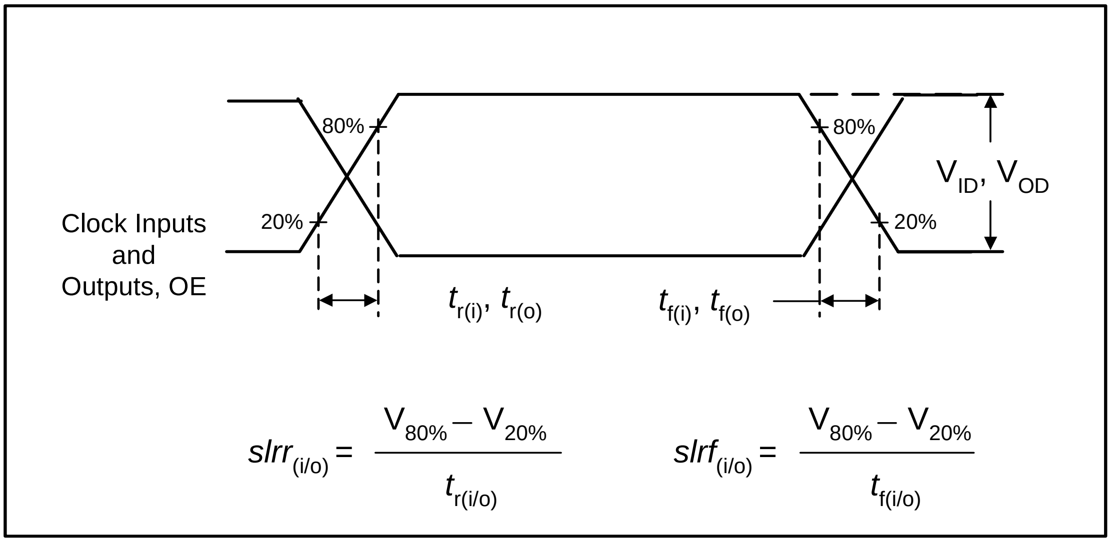


Figure 12 — Input and Output Slew Rates

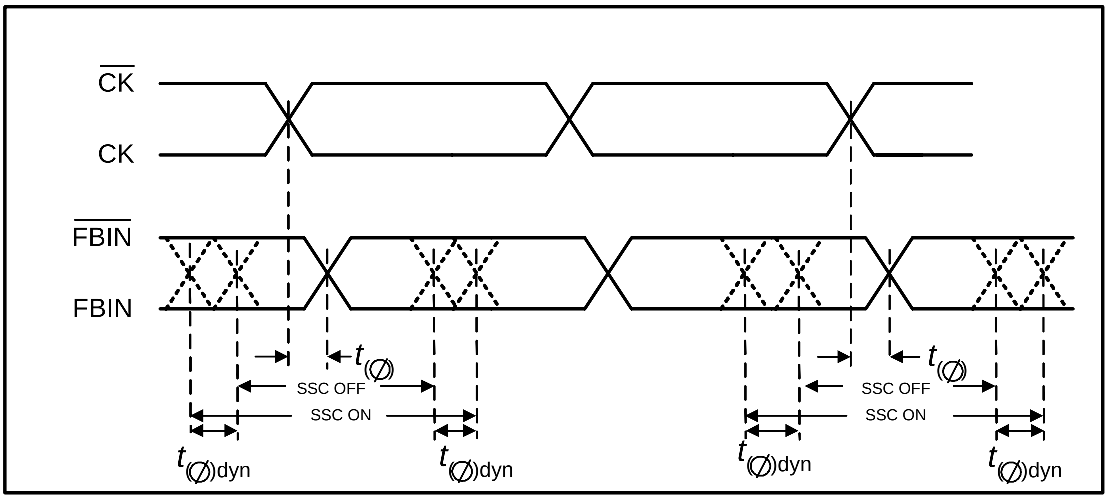


Figure 13 — Dynamic Phase Offset

5 Test circuit and switching waveforms (cont'd)

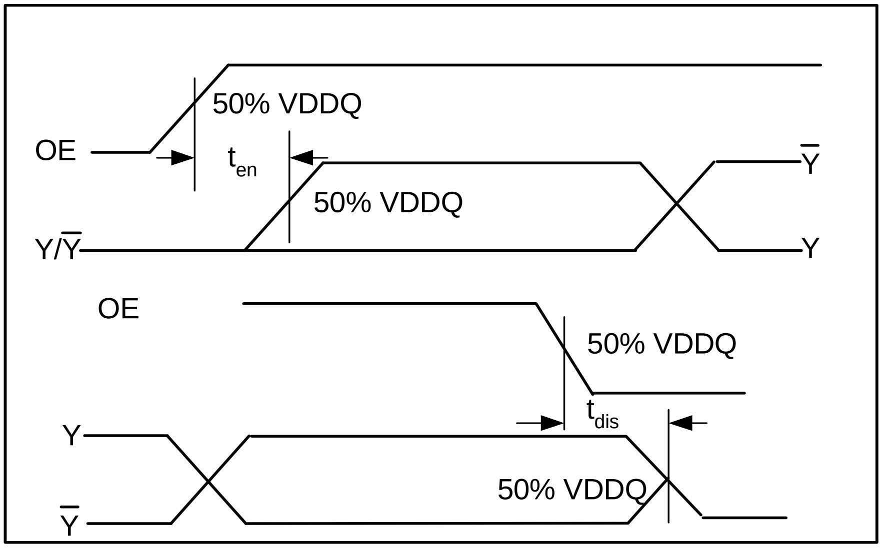


Figure 14 — Time delay between OE and Clock Output (Y, $\overline{Y}$)

6 Recommended Filtering for the Analog Power supply (AV_{DD})

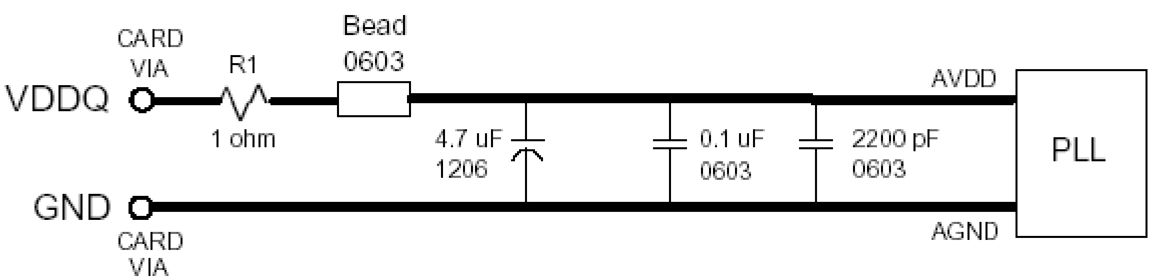


Figure 15 — AV_{DD} Filtering

- Place the 2200pF capacitor close to the PLL

- Use a wide trace for the PLL analog power & ground. Connect PLL & caps to AGND trace & connect trace to one GND via (farthest from PLL).

- Recommended bead: Fair-Rite P/N 2506036017Y0 or equivalent (0.8 Ohm DC max, 600 Ohms @ 100 MHz).

7 Reference to other applicable JEDEC standards and publications

JESD65, *Definition of Skew Specification for Standard Logic Devices*

JESD8-7, *1.8 Volt ±0.1 V (Normal Range), and 1.2 - 1.95V (Wide Range) Power Supply Voltage and Interface for Nonterminated Digital Integrated Circuits.*

JESD8-15, *Stub Series Terminated Logic for 1.8 V (SSTL_18)*

JESD21-C, *Configuration for Solid State Memories*

JEDEC